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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/886,741	06/21/2001	Vincent Chan	ATI.0100680	6028

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Christopher J. Reckamp, Esq.
VEDDER, PRICE, KAUFMAN & KAMMHOLZ
222 North LaSalle Street
Chicago, IL 60601

EXAMINER
CHU, CHRIS C

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 11/18/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/886,741	CHAN ET AL.	
	Examiner	Art Unit	
	Chris C. Chu	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 October 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 20, 22 - 40 and 43 - 55* is/are pending in the application.

4a) Of the above claim(s) *7,10,12-14,19,22,24-40,48,50-52 and 55* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8,9,11,15-18,20, 23, 43-47, 49, 53 and 54* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Response to Amendment

1. Applicant's amendment filed on October 28, 2002 has been received and entered in the case.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1 ~ 6, 8, 9, 15 ~ 18, 20, 43 ~ 47, 49, 53 and 54 are rejected under 35 U.S.C. 102(b) as being anticipated by Fallon et al.

Regarding claim 1, Fallon et al. discloses in Fig. 46 a device comprising:

- a package module (874) including a substrate having a standard package footprint;
- an unpackaged semiconductor die (864) directly attached to the package module, the unpackaged semiconductor die encapsulated (876) onto the package module in a structure having a substantially rectangular footprint; and
- a packaged semiconductor (862) attached to the multi-die module.

Regarding claim 2, Fallon et al. discloses in Fig. 46 the packaged semiconductor (862) being packaged in a ball grid array package.

Regarding claim 3, since Fallon et al. does not limit the unpackaged semiconductor die to any particular or specific device, hence his/her disclosure encompasses all well known semiconductor die's including a "graphics-processor."

Regarding claim 4, since Fallon et al. does not limit the packaged semiconductor die to any particular or specific device, hence his/her disclosure encompasses all well known semiconductor die's including a "memory."

Regarding claim 5, Fallon et al. discloses in column 37, lines 47 and 48 a plurality of packaged semiconductors (862) being attached to the package module.

Regarding claim 6, Fallon et al. discloses in Fig. 46 the unpackaged semiconductor die (864) being wire (868) bonded to the package module.

Regarding claims 8 and 20, the phrase "wherein attached includes surface-mount technology reflow" is product-by-process limitation. Even though product-by-process claims are limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process. In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985) (citations omitted). A "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, **190 USPQ 15 at 17** (footnote 3). See also In re Brown, **173 USPQ 685**: In re Luck, **177 USPQ 523**; In re Fessmann, **180 USPQ 324**: In re Avery, **186 USPQ 116**; In re Wertheim, **191 USPQ 90 (209 USPQ 254** does not deal

with this issue); and In re Marosi et al., **218 USPQ 289** final product per se which must be determined in a "product by, all of" claim, and not the patentability of the process, and that an old or obvious product, whether claimed in "product by process" claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

Regarding claim 9, Fallon et al. discloses in Fig. 46 the encapsulated structure (876) having a footprint greater than the footprint of the unpackaged semiconductor die (864).

Regarding claim 15, Fallon et al. discloses in Fig. 46 a device comprising:

- a package module (874);
- a die (864) directly attached to the package module, the die encapsulated (876) on the package module in a structure having a rectangular footprint; and
- a die (864) directly attached to the package module; and
- a packaged die (862) attached to the package module.

Further, the phrase "sized to be interchangeable with standard package sizes" is intended use language which does not differentiate the claimed apparatus from Fallon et al. Furthermore, since Fallon et al. does not limit the unpackaged semiconductor die to be any particular or specific device, hence his/her disclosure encompasses all well known semiconductor die's including a "graphics-processor die." Finally, since Fallon et al. does not limit the packaged semiconductor die to be any particular or specific device, hence his/her disclosure encompasses all well known semiconductor die's including a "memory die."

Regarding claim 16, Fallon et al. discloses in Fig. 46 the packaged memory (862) being packaged in a ball grid array package.

Regarding claim 17, Fallon et al. discloses in column 37, lines 47 and 48 a plurality of packaged memory (862) being attached to the package module.

Regarding claim 18, Fallon et al. discloses in Fig. 46 directly attached including the graphics processing die (864) being wire (868) bonded to the packaged module.

Regarding claim 43, Fallon et al. discloses in Fig. 46 a multi-die module, comprising :

- a substrate (874) having a first surface and a second surface;
- an unpackaged semiconductor die (864) mounted to the first surface of the substrate, the semiconductor die encapsulated (876) in a structure having a rectangular footprint; and
- a packaged semiconductor die (862) mounted on the first surface of the substrate.

Regarding claim 44, Fallon et al. discloses in column 37, lines 47 and 48 a second packaged semiconductor die mounted on the first surface of the substrate.

Regarding claim 45, Fallon et al. discloses in column 37, lines 48 and 49 a plurality of unpackaged semiconductor die mounted on the first surface of the substrate.

Regarding claim 46, Fallon et al. discloses in Fig. 46 the unpackaged semiconductor die being mounted to the first surface of the substrate by wire (868) bonding.

Regarding claim 47, Fallon et al. discloses in Fig. 46 and column 37, line 64 the encapsulating structure (876) being further comprised of an encapsulating material including epoxy, metal cap or silicon coatings.

Regarding claim 49, Fallon et al. discloses in Fig. 46 each of the unpackaged semiconductor die and packaged semiconductor die having a top surface, and wherein the top

surfaces of the unpackaged semiconductor die and the packaged semiconductor die being of substantially equal distance from the first surface of the substrate.

Regarding claim 53, since Fallon et al. does not limit the unpackaged semiconductor die to be any particular or specific device, hence his/her disclosure encompasses all well known semiconductor die's including a "graphics-processor."

Regarding claim 54, since Fallon et al. does not limit the packaged semiconductor die to be any particular or specific device, hence his/her disclosure encompasses all well known semiconductor die's including a "memory."

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 11 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fallon et al. in view of Takano et al.

Regarding claims 11 and 23, Fallon et al. discloses the semiconductor package set forth in the claims except for the standard package sizes being 40mm X 40mm. However, Takano et al. discloses in TABLE 1 a standard package sizes being 40mm X 40mm. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to

modify Fallon et al. by using the standard package sizes as taught by Takano et al. The ordinary artisan would have been motivated to modify Fallon et al. in the manner described above for at least the purpose of reducing a limitation in the size of a semiconductor chip (column 2, lines 6 and 7).

Response to Arguments

6. Applicant's arguments filed on October 28, 2002 have been fully considered but they are not persuasive.

On page 4, applicant argues "[T]he Applicants traverse the withdrawal of claims 7 and 19 from consideration as '... flip-chip attachment ...' as recited in each of the aforementioned claims does in fact read on Fig. 5. The Examiner's attention is directed, for example, to page 5, lines 2-5 of the originally filed specification which provides support ... Thus, as the originally filed specification and figures provide support for '... flip-chip attachment ...' as recited in claims 7 and 19, the Applicants submit that such claims do read on the embodiment illustrated in Fig. 5, and that the withdrawal of claims 7 and 19 is improper. Accordingly, reconsideration of the withdrawal of claims 7 and 19 from consideration is respectfully requested." Since Fig. 5 of instant invention does not show the following limitation of claims 7 and 19 "the **unpackaged** semiconductor die is attached to the package module by flip-chip attachment," the argument is not persuasive. Further, the originally filed specification, specifically, on page 5, lines 2-5 does not disclose the **unpackaged** semiconductor die being attached by flip-chip attachment.

Further, applicant argues "Fig. 46 does not illustrate and the corresponding portion of the specification do not describe, for example, the wire bond chip as being encapsulated within a structure having a substantially rectangular footprint. In fact, no encapsulation structure is illustrated in Fig. 46." The argument is not persuasive. Fallon et al. clearly discloses in Fig. 46 encapsulation structure (876) encapsulated the wire bond chip (864). Further, Fallon et al. discloses a structure (874) having a substantially rectangular footprint (see Fig. 41).

Furthermore, applicant argues "the wire bond chip does not appear to be '... directly attached ...' to the underlying substrate as defined in claim 1, as the wire bond chip is actually attached to a metal structure (710)." The argument is not persuasive because Fallon et al. clearly discloses in Fig. 32 and column 35, lines 24 ~ 42 that the metal structure (710) is a flat metal pads of the wiring layer (706) for connecting a flip chip (716) to a base (698). Thus, it is clear that the metal structure (710) in Fig. 46 is not attached to the wire bond chip. Therefore, Fallon et al. discloses in Fig. 46 an unpackaged semiconductor die (864) is directly attached to the package module (874).

Finally, in response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

For the above reasons the rejection is maintained.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is (703) 305-6194. The examiner can normally be reached on M-F (10:30 - 7:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7382 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Chris C. Chu
Examiner
Art Unit 2815

c.c.
November 7, 2002

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800